



FIG. 1 (a)

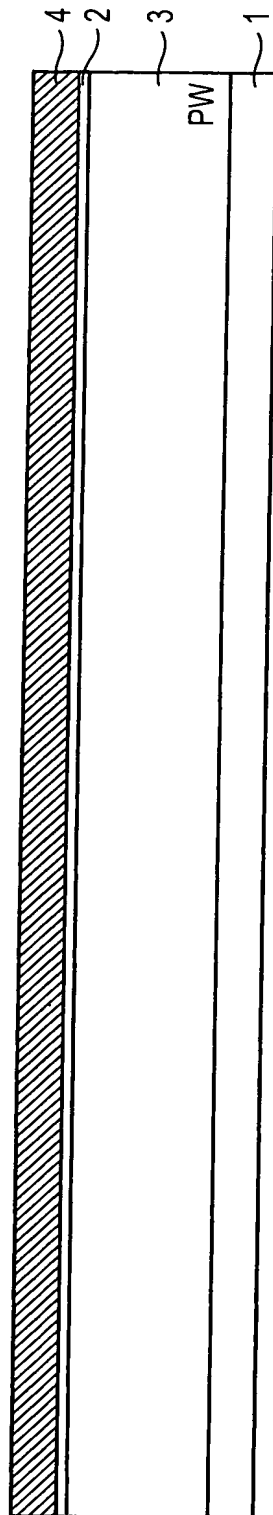
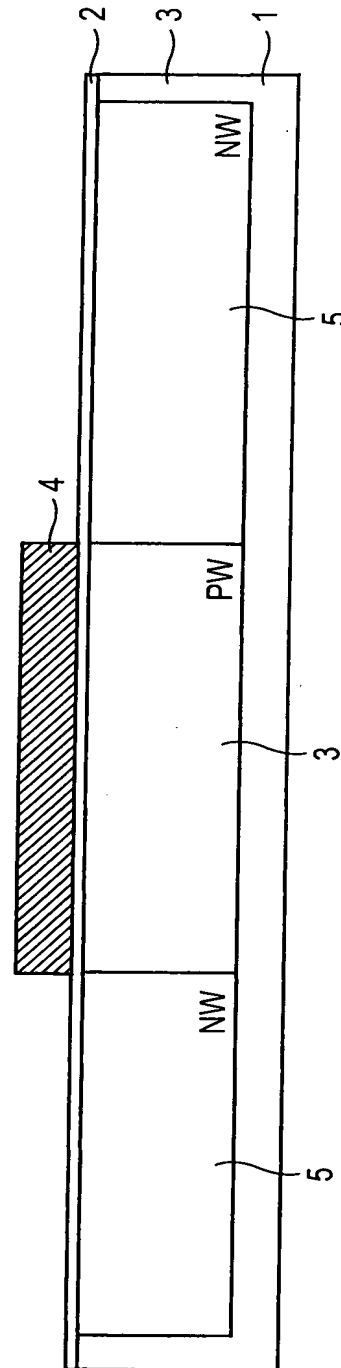


FIG. 1 (b)



2/14

FIG. 2 (a)

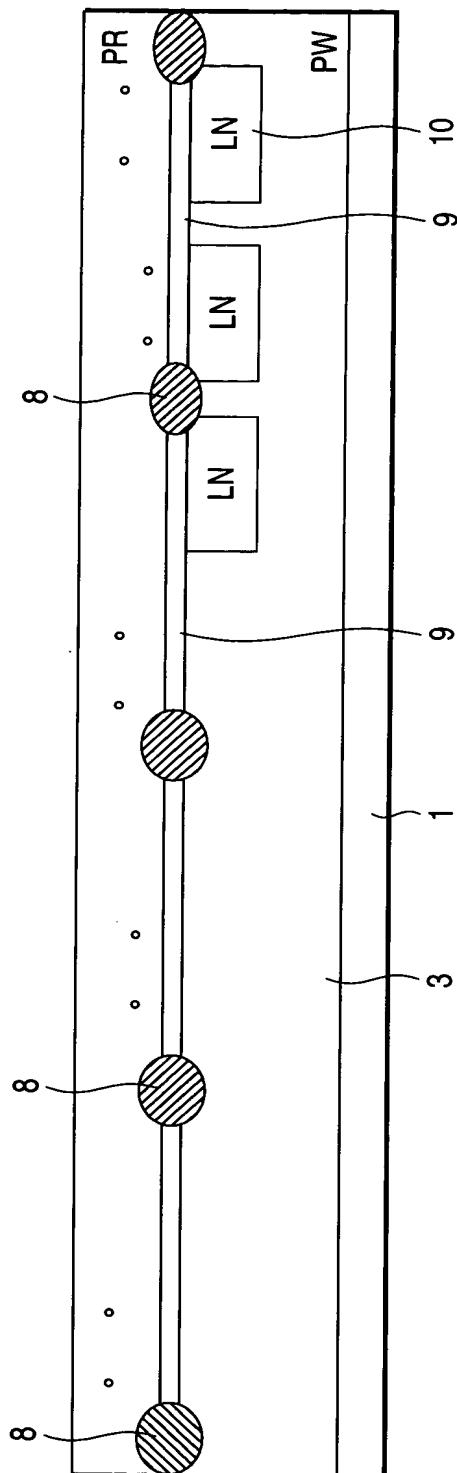
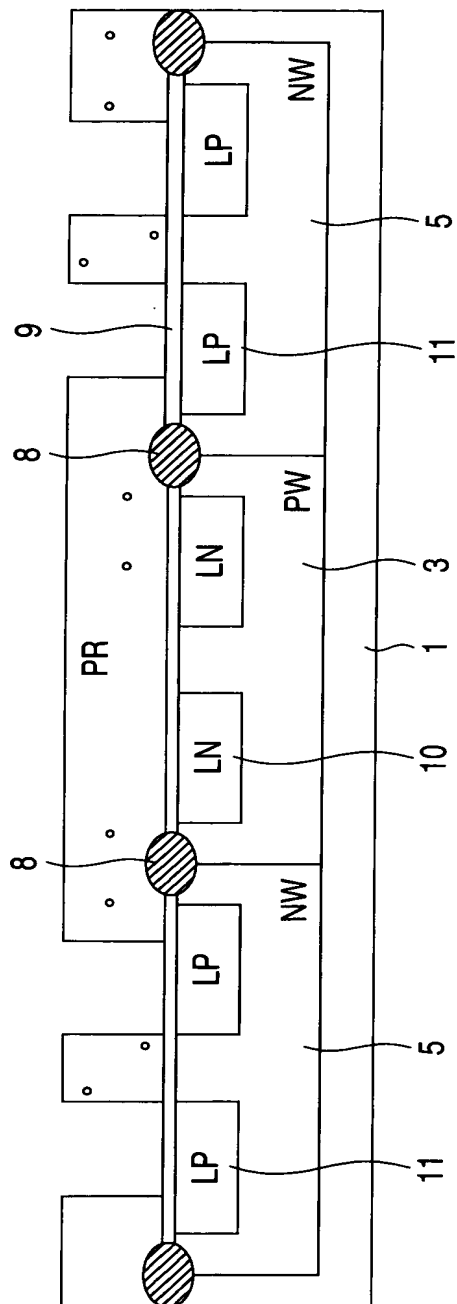


FIG. 2 (b)



3/14

FIG. 3 (a)

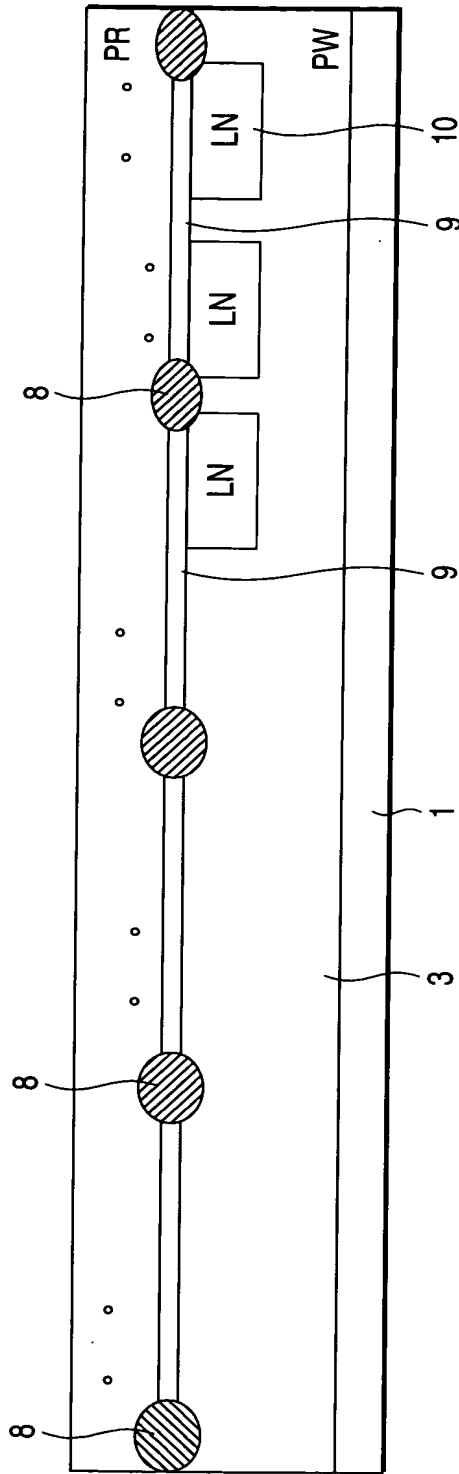
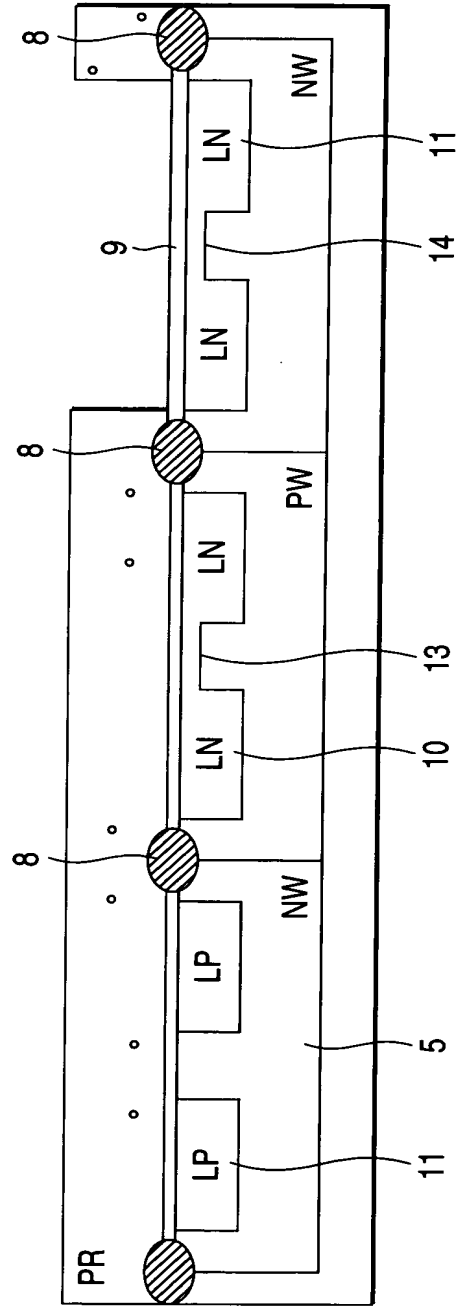


FIG. 3 (b)



4/14

FIG. 4 (a)

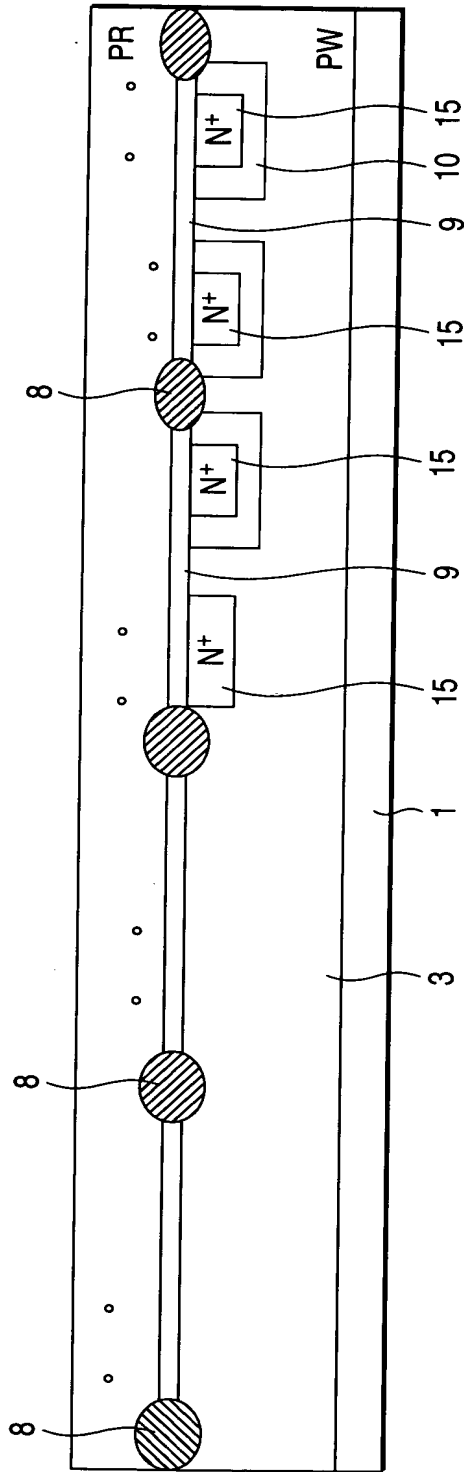
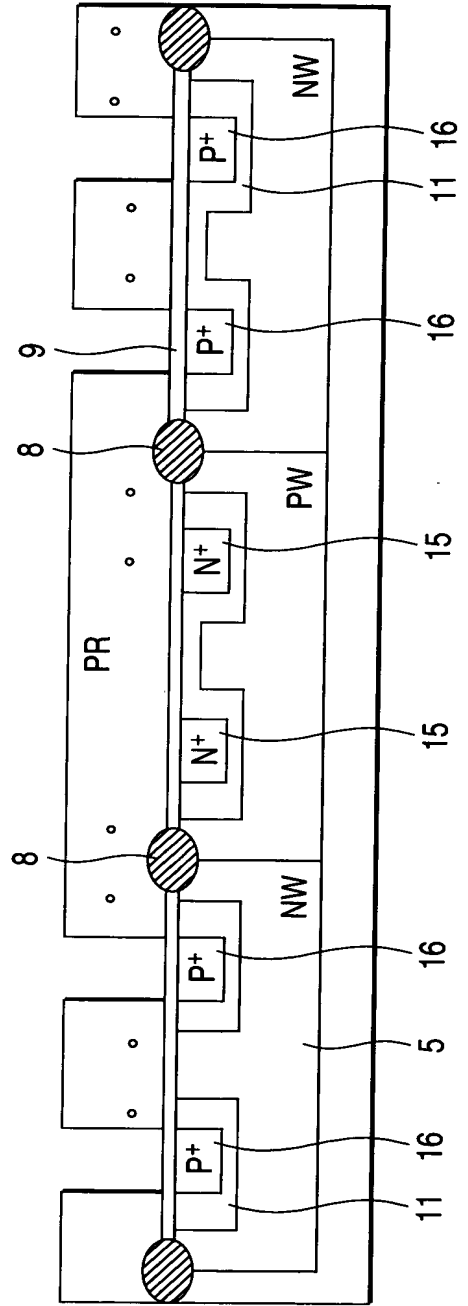


FIG. 4 (b)



5/14

FIG. 5 (a)

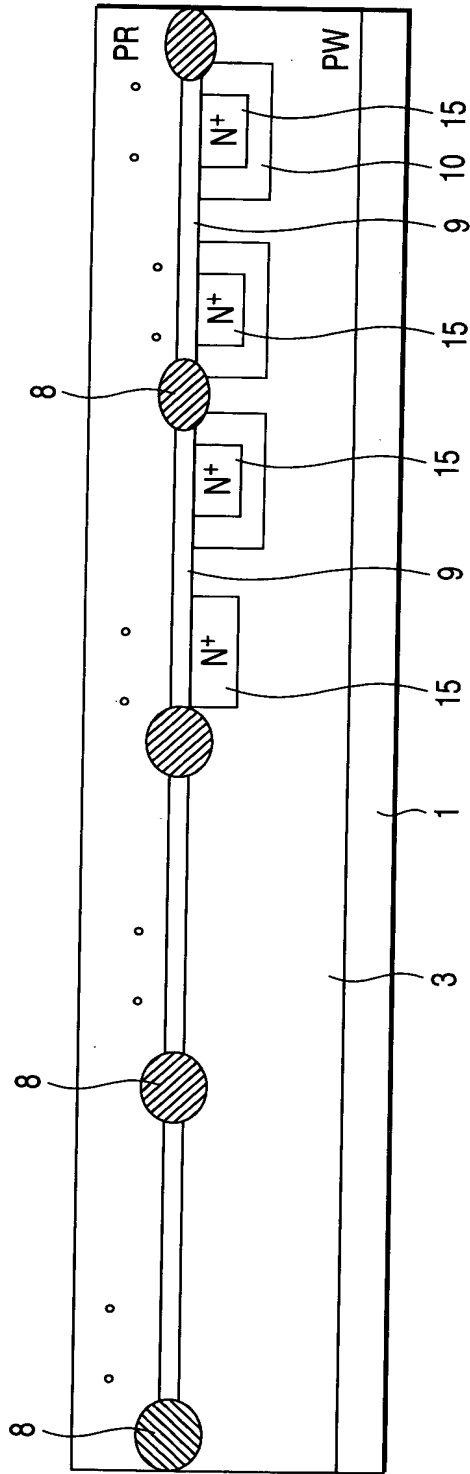
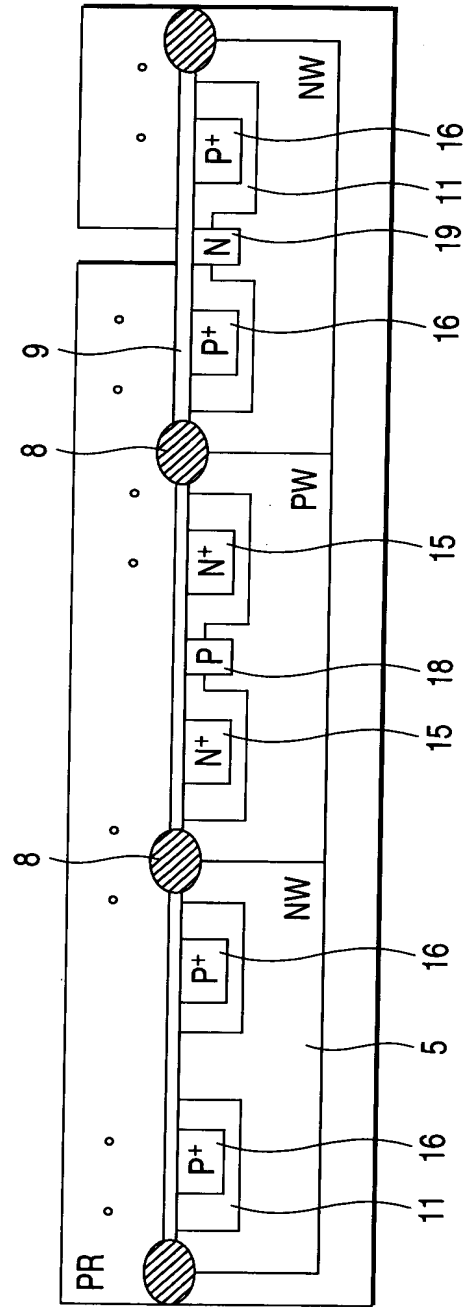


FIG. 5 (b)



This diagram shows a cross-sectional view of a semiconductor device. A central channel (1) is formed in a substrate (21). The channel is flanked by two regions (22) and is covered by a gate layer (3). The gate layer is divided into four segments (9) by three gate spacers (15). Each gate segment is connected to a common gate terminal (8) on the left. The gate spacers are connected to a common source/drain terminal (8) on the right. The device is labeled with 'PR' (Passivation) on the left, 'SNW' (Source/Drain) on the right, and 'PW' (Passivation) on the right. The channel is labeled '1', the gate segments are labeled '9', the gate spacers are labeled '15', and the substrate is labeled '21'.



8/14

FIG. 8 (a)

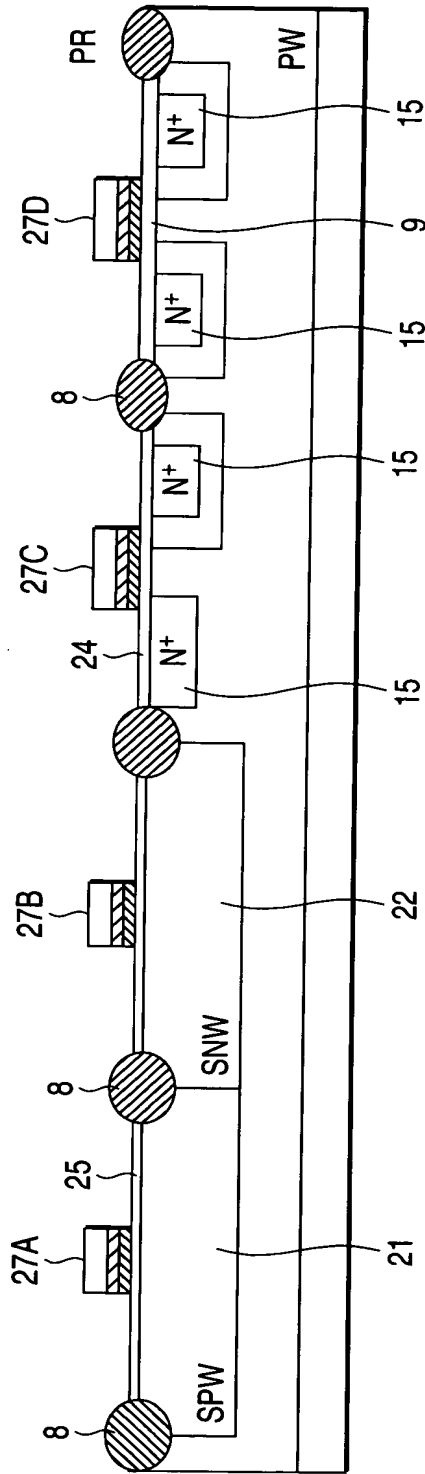
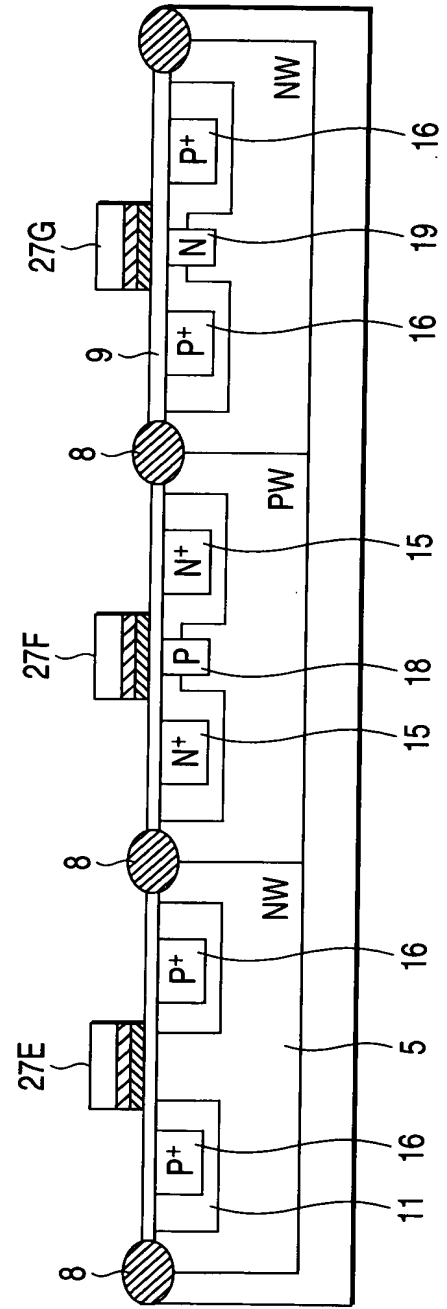


FIG. 8 (b)





9/14

FIG. 9 (a)

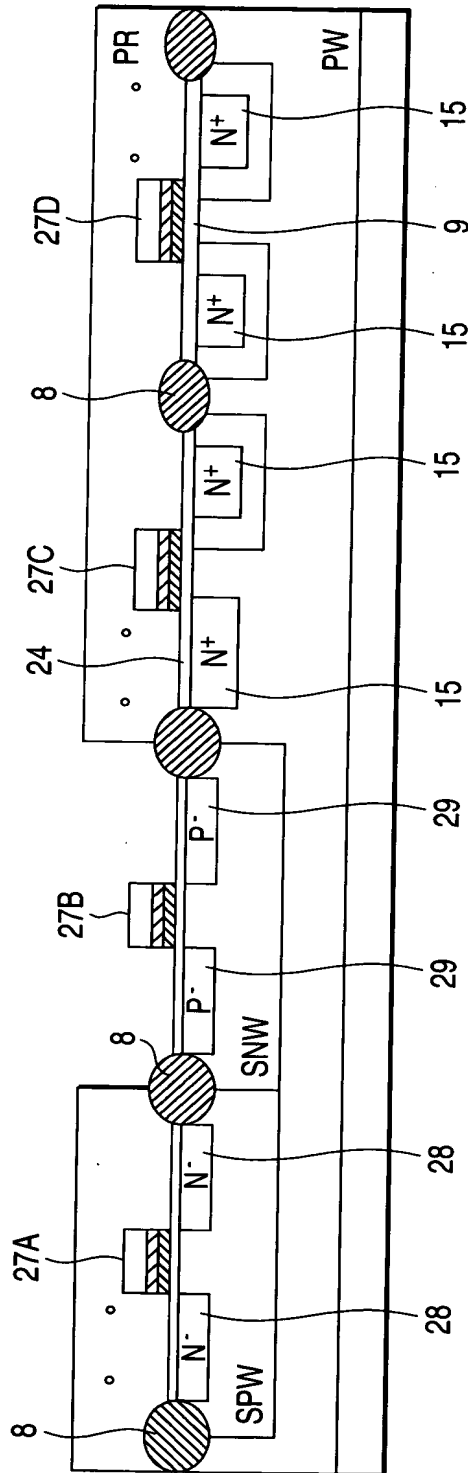
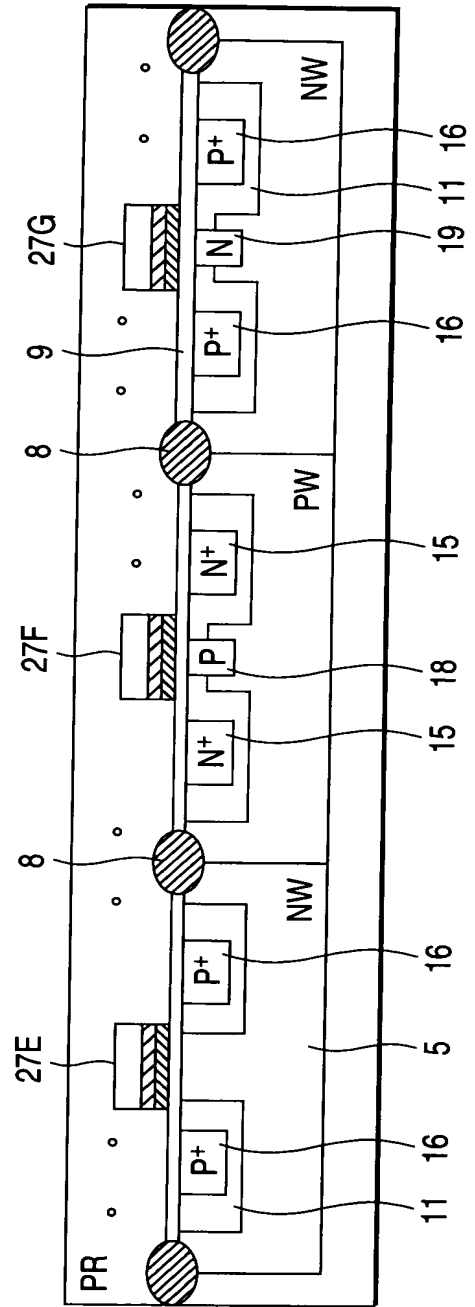


FIG. 9 (b)



10/14

FIG. 10 (a)

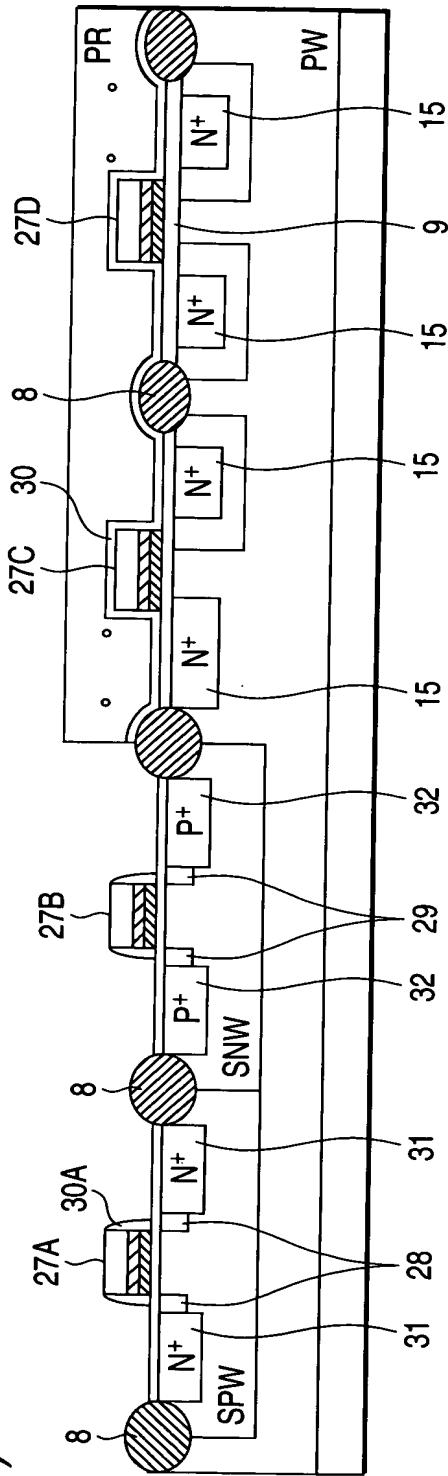
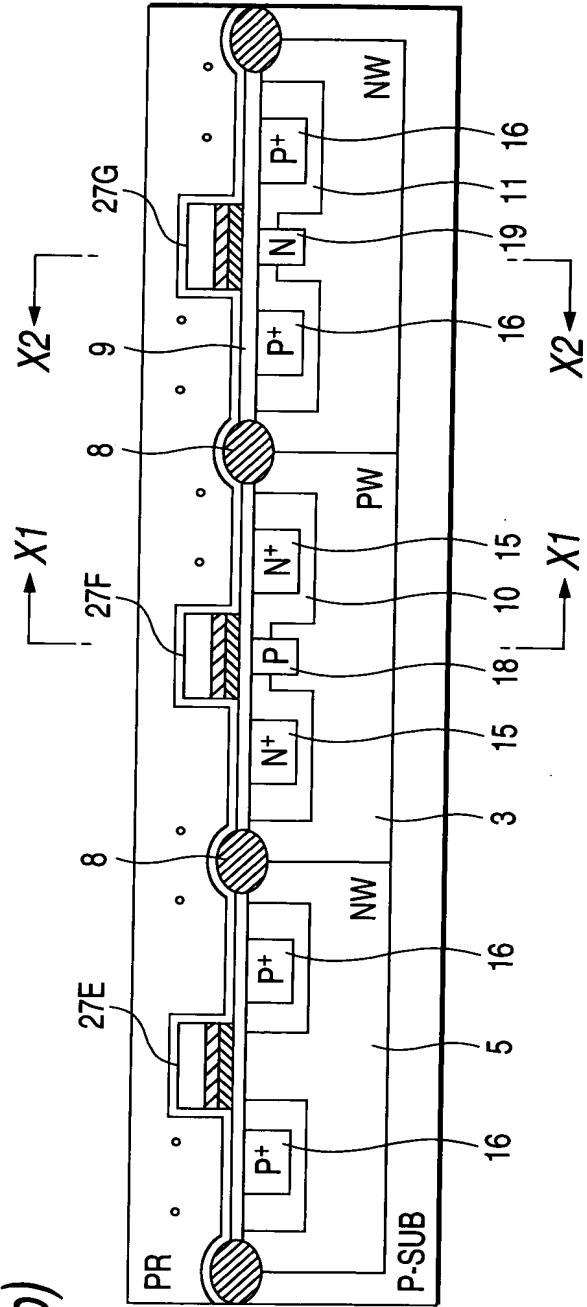


FIG. 10 (b)



11/14

FIG. 11 (a)

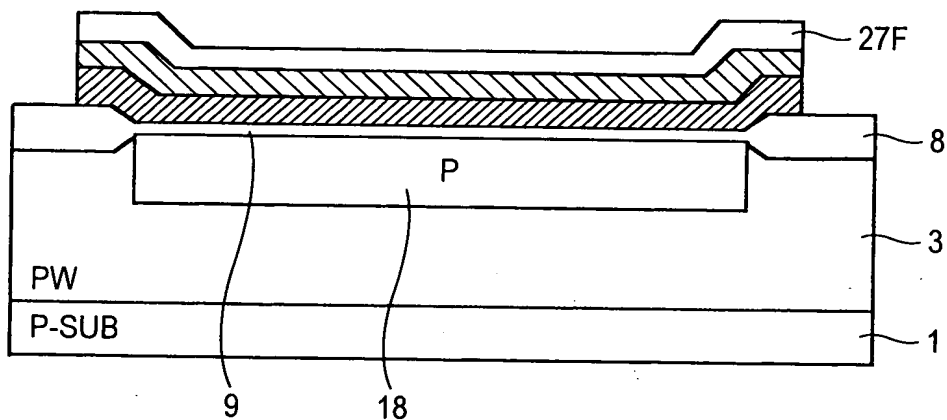
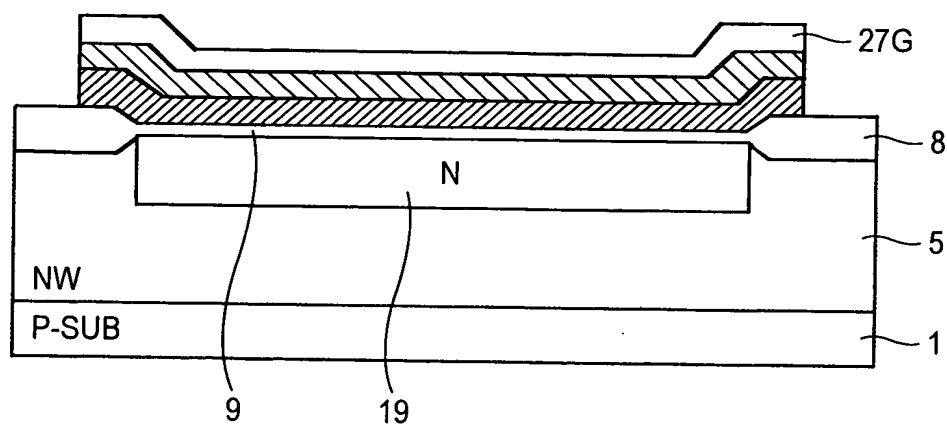


FIG. 11 (b)



12/14

FIG. 12 (a)

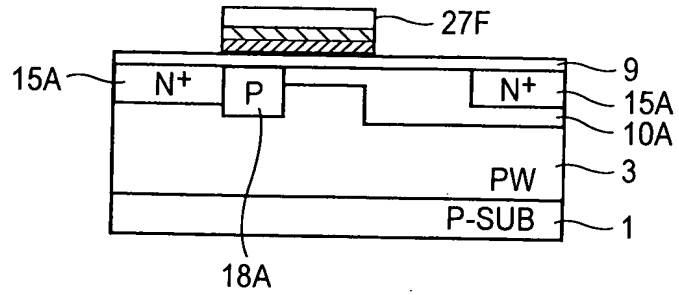
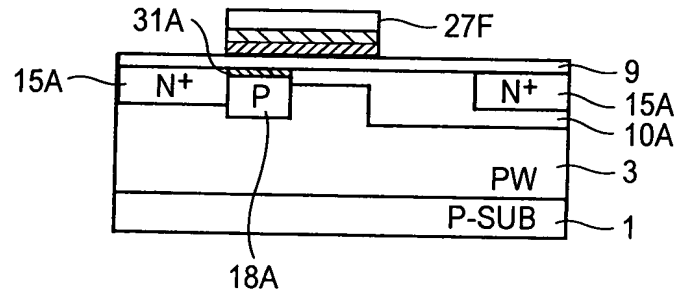


FIG. 12 (b)



13/14

FIG. 13 (a)

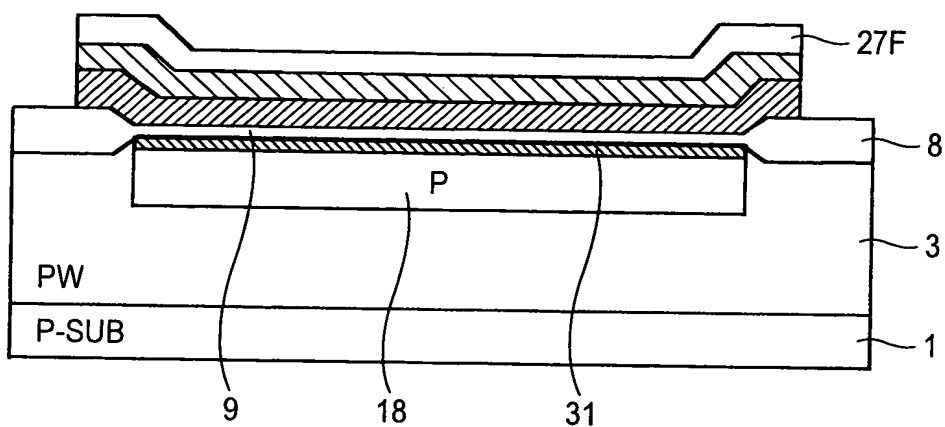
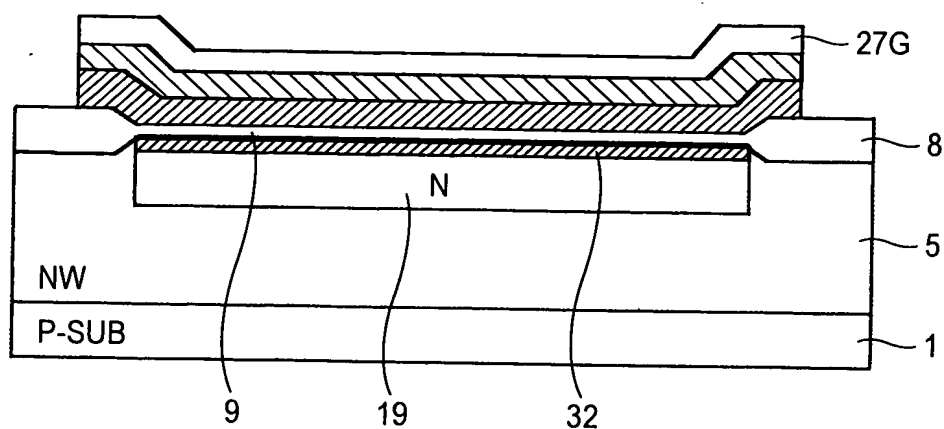


FIG. 13 (b)



14/14

FIG. 14

